AN-9719

Applying Fairchild Power Switch (FPS™) FSL1x7 to Low- Power Supplies

1. Introduction

The highly integrated FSL-series consists of an integrated current-mode Pulse Width Modulator (PWM) and an avalanche-rugged 700V SenseFET. It is specifically designed for high-performance offline Switched Mode Power Supplies (SMPS) with minimal external components.

The features of the integrated PWM controller include a proprietary green-mode function providing off-time modulation to linearly decrease the switching frequency at light-load conditions to minimize standby power consumption. The PWM controller is manufactured using the BiCMOS process to further reduce power consumption. The green mode and burst mode functions with a low operating current (2mA in green mode) maximize light-load efficiency so that the power supply can meet stringent standby power regulations.

The FSL-series has a built-in synchronized slope compensation to achieve stable peak-current-mode control. The proprietary external line compensation ensures constant output power limit over a wide AC input voltage range, $90V_{AC}$ to $264V_{AC}$, and helps optimize the power stage.

Many protection functions; such as open–loop / overload protection (OLP), over-voltage protection (OVP), and over-temperature protection (OTP); are fully integrated into FSL-series. These features improve the SMPS reliability without increasing system cost.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSL-series reduces total component count, converter size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform for design of cost-effective flyback converters.

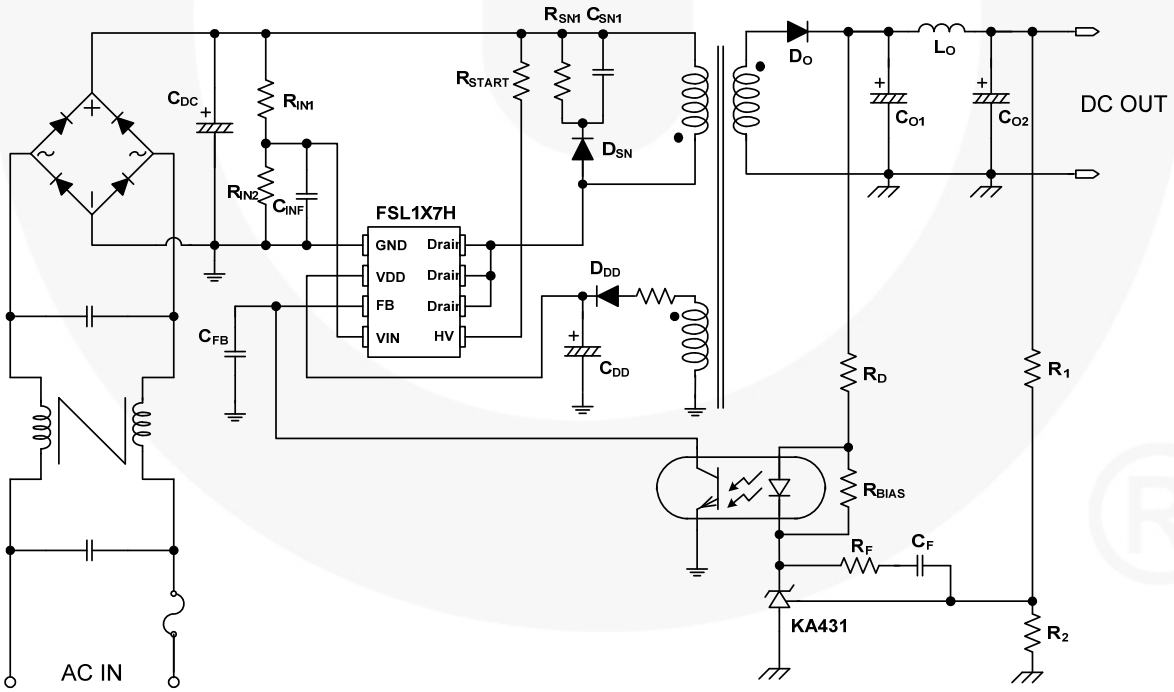

Figure 1. Typical Application Circuit

2. Device Block Description

2.1 Startup Circuit

For startup, the HV pin is connected to the line input or bulk capacitor through external resistor R_{HV}, as shown in Figure 2. Typical startup current is 3.5mA and it charges the V_{DD} capacitor (C_{DD}) through resistor R_{HV}. The startup current turns off when the V_{DD} capacitor voltage reaches V_{DD-ON}. The V_{DD} capacitor maintains V_{DD} until the auxiliary winding of the transformer provides the operating current.

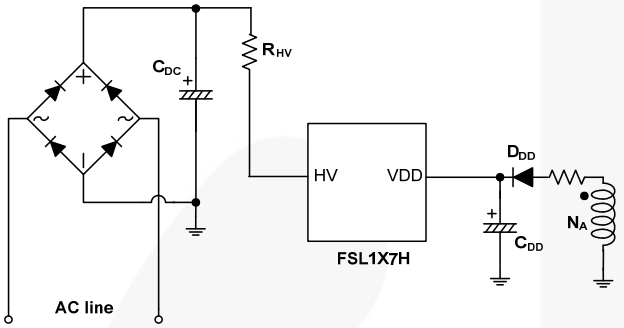

Figure 2. Startup Circuit

2.2 Soft-Start

The FSL-series has internal soft-start circuit that slowly increases the SenseFET current during startup. The typical soft-start time is 5ms, during which the V_{Limit} level is increased in six steps to smoothly establish the required output voltage, as shown in Figure 3. It also helps prevent transformer saturation and reduce stress on the secondary diode during startup.

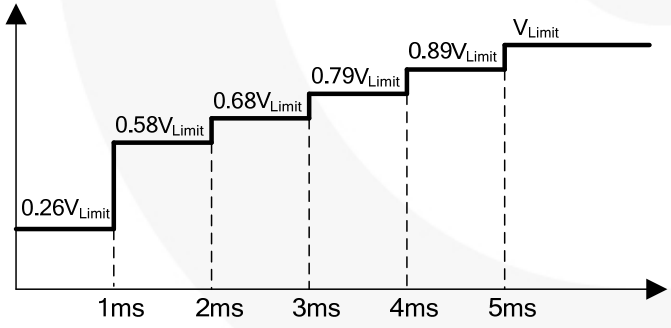

Figure 3. Soft-Start Function

2.3 Green Mode Operation

The FSL-series uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 4, such that the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 100kHz. Once V_{FB} decreases below V_{FB-N} (2.5V), the PWM frequency starts to linearly decrease from 100kHz to 18kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.4V), the switching frequency is fixed at 18kHz and FSL-series enters "deep" green mode to reduce the standby power consumption. As V_{FB} decreases below V_{FB-ZDC} (2.1V), FSL-series enters into burst-mode operation. When V_{FB} drops below V_{FB-ZDC}, FSL-series stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above V_{FB-ZDC}, switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss to improve power saving, as shown in Figure 5.

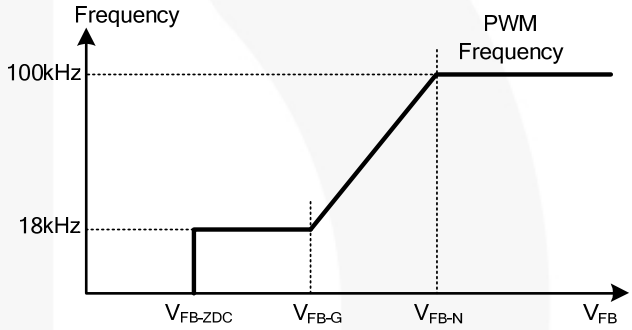

Figure 4. PWM Frequency

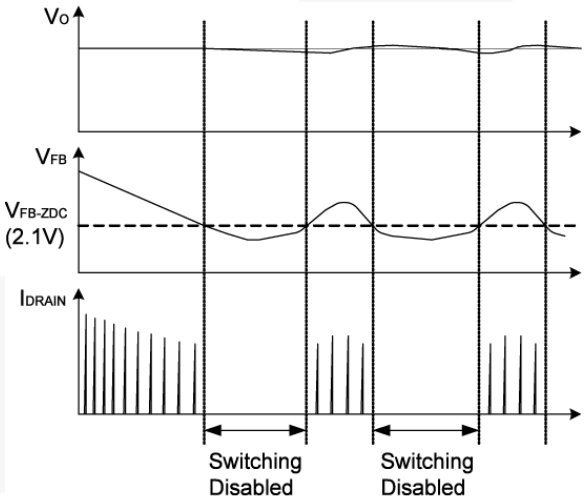

Figure 5. Bust-Mode Operation

2.4 Constant Power Control

To constantly limit the output power of the converter, high / low line compensation is included. Sensing the converter input voltage through the VIN pin, the high / low line compensation function generates a line-voltage-dependent peak-current-limit threshold voltage for constant power control, as shown in Figure 6.

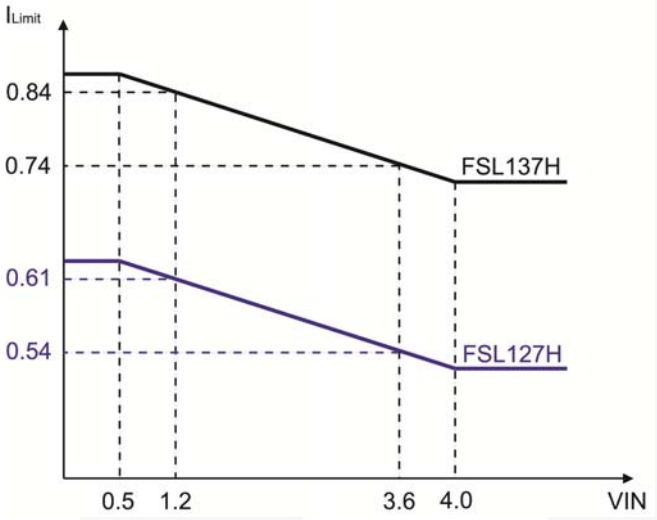

Figure 6. Constant Power Control

2.5 Protection Functions

The FSL-series provides full protection functions to prevent the power supply and the load from being damaged. The protection features is shown in Table 1.

Table 1. Protection Functions

	FSL127H	FSL137H
OVP	Latch	Latch
OTP	Latch	Latch
OLP	Auto Restart	Auto Restart
VIN-H	Latch	Latch
VIN-L	Auto Restart	Auto Restart

2.5.1 V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage caused by over voltage on the V_{DD} pin. The OVP is triggered when V_{DD} reaches 28V. It has debounce time (typically 130µs) to prevent false trigger by switching noise.

2.5.2 Over-Temperature Protection (OTP)

The SenseFET and the control IC integration make temperature detection of the SenseFET easier. When the junction temperature exceeds approximately 142°C, thermal shutdown is activated.

2.5.3 Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown) is open circuit, as shown in Figure 7, or an output over-current or short occurs; there is no current flowing through the opto-coupler transistor. V_{FB} (feedback voltage) pulls up to 6V. When the feedback voltage is above 4.6V for longer than 56ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value longer than 56ms due to the overload condition.

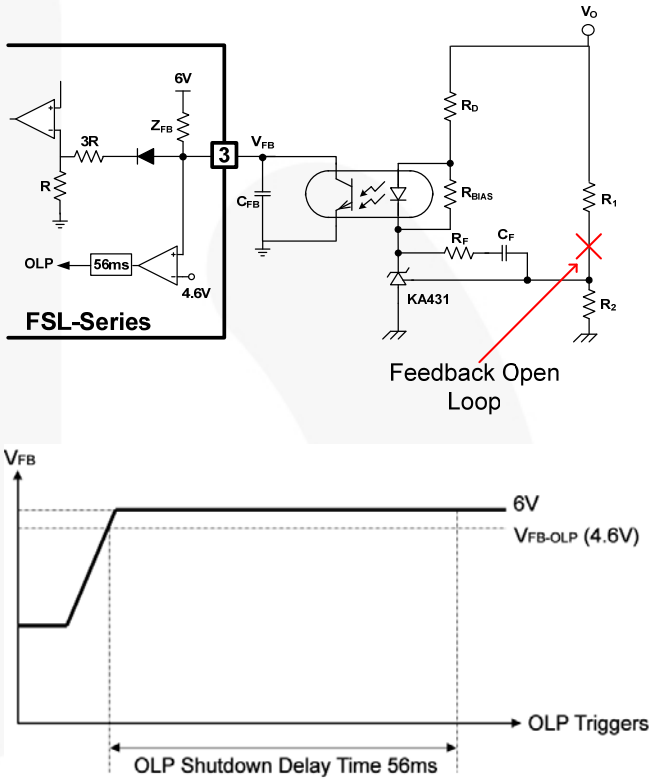

Figure 7. OLP Operator

3. Design Example

Flyback converters have two kinds of operation modes; Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Each has its own advantages and disadvantages. In general, DCM generates lower stress for the rectifier diodes, since the diodes are operating at zero current just before becoming reverse biased and the reverse recovery loss is minimized. The transformer size can be reduced using DCM because the average energy storage is low compared to CCM. However, DCM causes high RMS current, which severely increases the conduction loss of the MOSFET for low line condition. For standby auxiliary power supply applications with low output voltage and minimal reverse recovery of Schottky diode, it is typical to design the converter such that the converter operates in CCM to maximize efficiency.

This section presents a design procedure using the Figure 1 schematic as a reference. An offline SMPS with 12W nominal output power has been selected as the example.

[STEP-1] Define the System Specifications

When designing a power supply, the following specifications should be determined first:

- Line Voltage Range ($V_{LINE^{MIN}}$ and $V_{LINE^{MAX}}$)
- Line Frequency (f_L)
- Nominal Output Power (P_O)
- Estimate Efficiencies for Nominal Load (η). The power conversion efficiency must be estimated to calculate the input power for nominal load condition. If no reference data is available, set η = 0.7~0.75 for low-voltage output applications and η = 0.8~0.85 for high-voltage output applications.

With the estimated efficiency, the input power for peak load condition is given by:

$$P_{IN} = \frac{P_O}{\eta} \quad (1)$$

(Design Example) The specifications of the target system are:

- $V_{LINE^{MIN}} = 90V_{RMS}$ $V_{LINE^{MAX}} = 264V_{RMS}$
- Line frequency (f_L) = 60Hz
- Nominal output power (P_O) = 12W (12V/1A)
- Estimated efficiency (η) = 0.8

$$P_{IN} = \frac{P_O}{\eta} = \frac{12}{0.8} = 15W$$

[STEP-2] Determine Input Capacitor (C_{IN}) and Input Voltage Range

It is typical to select the input capacitor as 2~3μF per watt of peak input power for the universal input range (85-265V_{RMS}) and 1μF per watt of peak input power for the European input range (195V-265V_{RMS}). With the input capacitor chosen, the minimum input capacitor voltage at nominal-load condition is obtained as:

$$V_{IN^{MIN}} = \sqrt{2 \cdot (V_{LINE^{MIN}})^2 - \frac{P_{IN} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}} \quad (2)$$

where D_{CH} is the input capacitor charging duty ratio defined in Figure 8, which is typically about 0.2.

The maximum input capacitor voltage is given as:

$$V_{IN^{MAX}} = \sqrt{2} V_{LINE^{MAX}} \quad (3)$$

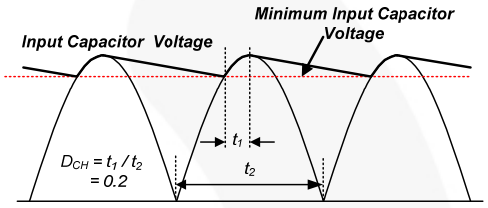

Figure 8. Input Capacitor Voltage Waveform

(Design Example) By choosing 20μF for input capacitor, the minimum input voltage for nominal load is obtained as:

$$V_{IN^{MIN}} = \sqrt{2 \cdot (V_{LINE^{MIN}})^2 - \frac{P_{IN} \cdot (1 - D_{CH})}{C_{IN} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{15 \cdot (1 - 0.2)}{20 \cdot 10^{-6} \cdot 60}} = 79V$$

The maximum input voltage is obtained as:

$$V_{IN^{MAX}} = \sqrt{2} \cdot V_{LINE^{MAX}} = \sqrt{2} \cdot 264 = 373V$$

[STEP-3] Determine the Reflected Output Voltage (V_{RO})

When the MOSFET is turned off, the input voltage (V_{IN}), together with the output voltage reflected to the primary (V_{RO}), are imposed across the MOSFET, as shown in Figure 9. With a given V_{RO}, the maximum duty cycle (D_{MAX}) and the nominal MOSFET voltage (V_{DS}^{NOM}) are obtained as:

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{IN^{MIN}}} \quad (4)$$

$$V_{DS^{NOM}} = V_{IN^{MAX}} + V_{RO} \quad (5)$$

$$V_{DO^{NOM}} = \frac{V_{IN^{MAX}} \cdot (V_O + V_F)}{V_{RO}} + V_O \quad (6)$$

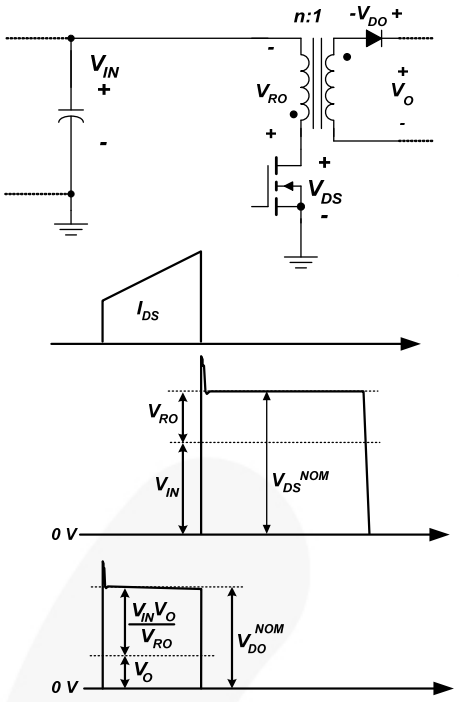

Figure 9. Output Voltage Reflected to the Primary

As can be seen in Equation 5, the voltage stress across MOSFET can be reduced by reducing V_{RO}. However, this increases the voltage stresses on the rectifier diodes in the secondary side, as shown in Equation 6. Therefore, V_{RO} should be determined by a balance between the voltage stresses of MOSFET and diode. Especially for low output voltage applications, the rectifier diode forward-voltage drop is a dominant factor determining the power supply efficiency. Therefore, the reflected output voltage should be determined such that rectifier diode forward voltage can be minimized. Table 2 shows the forward-voltage drop for Schottky diodes with different voltage rating.

The actual drain voltage and diode voltage rise above the nominal voltage is due to the leakage inductance of the transformer as shown in Figure 9. It is typical to set V_{RO} such that V_{DS}^{NOM} and V_{DO}^{NOM} are 70~80% of voltage ratings of MOSFET and diode, respectively.

Table 2. Diode Forward-Voltage Drop for Different Voltage Ratings (3A Schottky Diode)

Part Name	V_{RRM}	V_F
SB320	20V	0.5V
SB330	30V	
SB340	40V	
SB350	50V	0.74V
SB360	60V	
SB380	80V	0.85V
SB3100	100V	

(Design Example) As can be seen in Table 2, it is recommended to use rectifier diode with 100V voltage rating to maximize efficiency. Assuming that the nominal voltages of MOSFET and diode are less than 80% of their voltage rating, the reflected output voltage is given as:

$$V_{DO^{NOM}} = \frac{V_{IN^{MAX}} \cdot (V_O + V_F)}{V_{RO}} + V_O$$

$$= \frac{373 \cdot (12 + 0.85)}{V_{RO}} + 12 < 0.8 \cdot 100 = 80$$

$$\rightarrow V_{RO} > \frac{373 \cdot (12 + 0.85)}{68} = 70.5V$$

$$V_{DS^{NOM}} = V_{IN^{MAX}} + V_{RO} < 0.8 \cdot 700 = 560$$

$$\rightarrow V_{RO} < 560 - 373 < 187V$$

By determining V_{RO} as 74V,

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{IN^{MIN}}} = \frac{74}{74 + 79} = 0.48$$

$$V_{DS^{NOM}} = V_{IN^{MAX}} + V_{RO} = 373 + 74 = 447V$$

$$V_{DO^{NOM}} = \frac{V_{IN^{MAX}} \cdot (V_O + V_F)}{V_{RO}} + V_O$$

$$= \frac{373 \cdot (12 + 0.85)}{74} + 12 = 76.8V$$

[STEP-4] Determine the Transformer Primary-Side Inductance (L_M)

The transformer primary-side inductance is determined for the minimum input voltage and nominal-load condition. With the D_{MAX} from Step-3, the primary-side inductance (L_M) of the transformer is obtained as:

$$L_M = \frac{(V_{IN^{MIN}} \cdot D_{MAX})^2}{2 \cdot P_{IN} \cdot f_{SW} \cdot K_{RF}} \quad (7)$$

where f_{SW} is the switching frequency and K_{RF} is the ripple factor at minimum input voltage and nominal load condition, defined as shown in Figure 10.

For DCM operation, $K_{RF} = 1$, and, for CCM operation, $K_{RF} < 1$. The ripple factor is closely related to the transformer size and the RMS value of the MOSFET current. Even though the conduction loss in the MOSFET can be reduced by reducing the ripple factor, too small a ripple factor forces an increase in transformer size. When designing the flyback converter to operate in CCM, it is reasonable to set K_{RF} = 0.25-0.5 for the universal input range and K_{RF} = 0.4-0.8 for the European input range.

Once L_M is calculated from equation (7) after choosing K_{RF}, the peak and RMS current of the MOSFET for the minimum input voltage and nominal load condition are obtained as:

$$I_{DS^{PK}} = I_{EDC} + \frac{\Delta I}{2} \quad (8)$$

$$I_{DS^{RMS}} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{D_{MAX}}{3}} \quad (9)$$

where:

$$I_{EDC} = \frac{P_{IN}}{V_{IN^{MIN}} \cdot D_{MAX}} \quad (10)$$

and

$$\Delta I = \frac{V_{IN^{MIN}} \cdot D_{MAX}}{L_M \cdot f_{SW}} \quad (11)$$

$$K_{RF} = \frac{\Delta I}{2I_{EDC}}$$

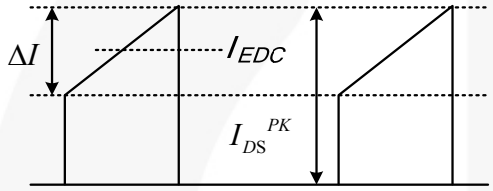

Figure 10. MOSFET Current and Ripple Factor (K_{RF})

(Design Example) Choosing the ripple factor as 0.88,

$$L_M = \frac{(V_{IN^{MIN}} \cdot D_{MAX})^2}{2 \cdot P_{IN} \cdot f_{SW} \cdot K_{RF}}$$

$$= \frac{(79 \cdot 0.48)^2}{2 \cdot 15 \cdot 100 \times 10^3 \cdot 0.88} \approx 540\mu H$$

$$I_{EDC} = \frac{P_{IN}}{V_{IN^{MIN}} \cdot D_{MAX}} = \frac{15}{79 \cdot 0.48} = 0.4A$$

$$\Delta I = \frac{V_{IN^{MIN}} \cdot D_{MAX}}{L_M \cdot f_{SW}} = \frac{79 \cdot 0.48}{540 \times 10^{-6} \cdot 100 \times 10^3} = 0.7A$$

$$I_{DS^{PK}} = I_{EDC} + \frac{\Delta I}{2} = 0.4 + 0.35 = 0.75A$$

$$I_{DS^{RMS}} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{D_{MAX}}{3}}$$

$$= \sqrt{[3(0.4)^2 + (0.35)^2]\frac{0.48}{3}} = 0.31A$$

[STEP-5] Choose the Proper FPS Considering Input Power and Peak Drain Current

With the resulting maximum peak drain current of the MOSFET (I_{DS}^{PK}) from Equation 8, choose the proper FPS for which the pulse-by-pulse current limit level (I_{LIM}) is higher than I_{DS}^{PK}. Since FPS has ±10% tolerance of I_{LIM}, there should be some margin when choosing the proper FPS device. The FSL-series lineup with proper power rating is summarized in Table 3.

Table 3. Lineup of FSL1x7-Series with Power Rating

Product	I_{LIM} at V_{IN}=1.2V			85-265V_{AC} Open Frame
	Min.	Typ.	Max.	
FSL127H	0.51A	0.61A	0.71A	16W
FSL137H	0.74A	0.84A	0.94A	19W

(Design Example)
$I_{DS^{PK}} = 0.75A < 0.84A(I_{LIM}\ Typ.)$
FSL137H is selected.

[STEP-6] Determine the Minimum Primary Turns

With a given magnetic core, the minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_{P^{MIN}} = \frac{L_M \cdot I_{LM}}{B_{SAT} \cdot A_e} \times 10^6 \quad (12)$$

where A_e is the cross-sectional area of the core in mm^2, I_{LIM} is the pulse-by-pulse current limit level, and B_{SAT} is the saturation flux density in Tesla.

The pulse-by-pulse current limit level is included in Equation 12 because the inductor current reaches the pulse-by-pulse current limit level during the load transient or overload condition. Figure 11 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density (B_{SAT}) decreases as temperature increases, the high-temperature characteristics should be considered. If there is no reference data, use B_{SAT} =0.3 T.

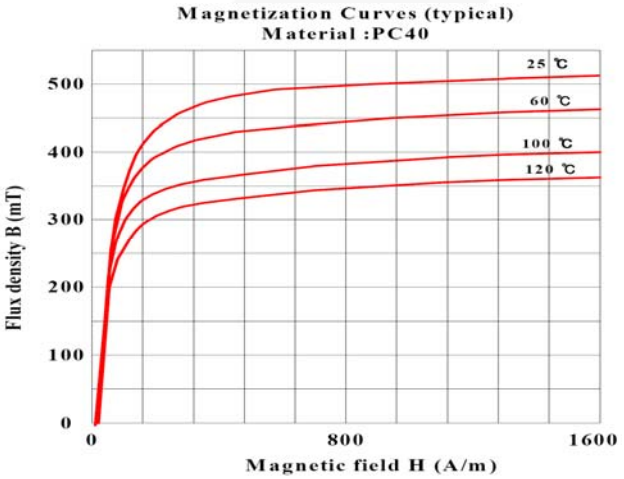

Figure 11.Typical B-H Characteristics of Ferrite Core (TDK/PC40)

(Design Example) EE-16 core is selected, whose effective cross-sectional area is 19.2mm^2. Choosing the saturation flux density as 0.3T, the minimum number of turns for the primary-side is obtained as:

$$N_{P^{MIN}} = \frac{L_M \cdot I_{LM}}{B_{SAT} \cdot A_e} \times 10^6$$

$$= \frac{540 \times 10^{-6} \cdot 0.8}{0.3 \cdot 19.2} \times 10^6 = 75$$

[STEP-7] Determine the Number of Turns for each Winding

Figure 12 shows a simplified diagram of the transformer. First calculate the turn ratio (n) between the primary-side and the secondary-side from the reflected output voltage (V_{RO}) determined in Step-3 as:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} \quad (13)$$

where N_P and N_S are the number of turns for primary-side and secondary-side, respectively; V_O is the output voltage; and V_F is the output diode (D_O) forward-voltage drop.

Next, determine the proper integer for N_S such that the resulting N_P is larger than N_P^{MIN} obtained from Equation 12.

The number of turns for the auxiliary winding for V_{DD} supply is determined as:

$$N_A = \frac{V_{DD^*} + V_{FA}}{V_O + V_F} \cdot N_{S1} \quad (14)$$

where V_{DD} is the supply voltage nominal value and V_{FA} is the forward-voltage drop of D_{DD} as defined in Figure 12.

Since V_{DD} increases as the output load increases, set V_{DD} at 5~8V higher than V_{DD} UVLO level (8V) to avoid the over-voltage protection condition during the peak-load operation.

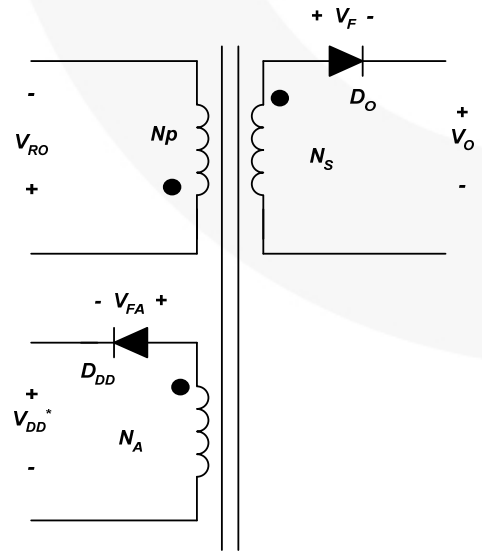

Figure 12. Simplified Transformer Diagram

(Design Example) Assuming the diode forward-voltage drop is 0.85V, the turn ratio is obtained as:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} = \frac{74}{12 + 0.85} = 5.8$$

Then determine the proper integer for N_S such that the resulting N_P is larger than N_P^{MIN} as:

$$N_S = 13,\ N_P = n \cdot N_S = 75 \geq N_{P^{MIN}}$$

Setting V_{DD^*} as 12V, the number of turns for the auxiliary winding is obtained as:

$$N_A = \frac{V_{DD^*} + V_{FA}}{V_O + V_F} \cdot N_{S1} = \frac{12 + 0.85}{12 + 0.5} \cdot 13 \approx 13$$

[STEP-8] Determine the Wire Diameter for Each Winding Based on the RMS Current of Winding

The maximum RMS current of the secondary winding is obtained as:

$$I_{SEC^{RMS}} = n \cdot I_{DS^{RMS}} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}} \quad (15)$$

The current density is typically 3~5A/mm^2 when the wire is long (>1m). When the wire is short with a small number of turns, a current density of 5~10A/mm^2 is acceptable. Avoid using wire with a diameter larger than 1mm to avoid severe eddy current or ac losses. For high-current output, it is better to use parallel windings with multiple strands of thinner wire to minimize skin effect.

(Design Example) The RMS current of primary-side winding is obtained from Step-4 as 0.31A. The RMS current of secondary-side winding is calculated as:

$$I_{SEC^{RMS}} = n \cdot I_{DS^{RMS}} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}}$$

$$= 5.8 \cdot 0.31 \sqrt{\frac{1 - 0.48}{0.48}} = 1.87A$$

0.3mm (5A/mm^2) and 0.4mm (8A/mm^2) diameter wires are selected for primary and secondary windings, respectively.

[STEP-9] Choose the Rectifier Diode in the Secondary-Side Based on the Voltage and Current Ratings

The maximum reverse voltage and the RMS current of the rectifier diode are obtained as:

$$V_{DO} = V_O + \frac{V_{IN^{MAX}}}{n} \quad (16)$$

$$I_{DO^{RMS}} = n \cdot I_{DS^{RMS}} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}} \quad (17)$$

The typical voltage and current margins for the rectifier diode are as follows:

$$V_{RRM} > 1.2 \cdot V_{DO} \quad (18)$$

$$I_F > 1.8 \cdot I_{DO^{RMS}} \quad (19)$$

where V_{RRM} is the maximum reverse voltage and I_F is the current rating of the diode.

(Design Example) The diode voltage and current are calculated as:

$$V_{DO} = V_O + \frac{V_{IN^{MAX}}}{n} = 12 + \frac{373}{5.8} = 76.3V$$

$$I_{DO^{RMS}} = n \cdot I_{DS^{RMS}} \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}}$$

$$= 5.8 \cdot 0.31 \sqrt{\frac{1 - 0.48}{0.48}} = 1.87A$$

5A and 100V diodes in parallel are selected for the rectifier diode.

[STEP-10] Feedback Circuit Configuration

Since FSL-series employs current-mode control, the feedback loop can be implemented with a one-pole and one-zero compensation circuit.

The current control factor of FPS, *K,* is defined as:

$$K = \frac{I_{LIM}}{V_{FB^{SAT}}} = \frac{I_{LIM}}{2.5} \quad (20)$$

where I_{LIM} is the pulse-by-pulse current limit and V_{FB}^{SAT} is the feedback saturation voltage, typically 2.5V.

As described in Step-4, it is typical to design the flyback converter to operate in CCM for heavy-load condition. For CCM operation, the control-to-output transfer function of a flyback converter using current mode control is given by:

$$G_{VC} = \frac{\hat{V}_O}{\hat{V}_{FB}} \quad (21)$$

$$= \frac{K \cdot R_L \cdot V_{IN}(N_P/N_S)}{2V_{RO} + V_{IN}} \cdot \frac{(1 + s/\omega_Z)(1 - s/\omega_{RZ})}{(1 + s/\omega_P)}$$

where R_L is the load resistance.

The pole and zeros of Equation 21 are obtained as:

$$\omega_Z = \frac{1}{R_C C_O}, \omega_{RZ} = \frac{R_L(1-D)^2}{DL_M(N_S/N_P)^2} \text{ and } \omega_P = \frac{(1+D)}{R_L C_O} \quad (22)$$

*w*here *D* is the duty cycle of the FPS and R_C is the ESR of C_O.

Notice that there is a right-half-plane (RHP) zero (ω_{RZ}) in the control-to-output transfer function of Equation 21. Because the RHP zero reduces the phase by 90 degrees, the crossover frequency should be placed below the RHP zero.

Figure 13 shows the variation of a CCM flyback converter control-to-output transfer function for different input voltages. This figure shows the system poles and zeros with the DC gain change for different input voltages. The gain is highest at the high input voltage condition and the RHP zero is lowest at the low input voltage condition.

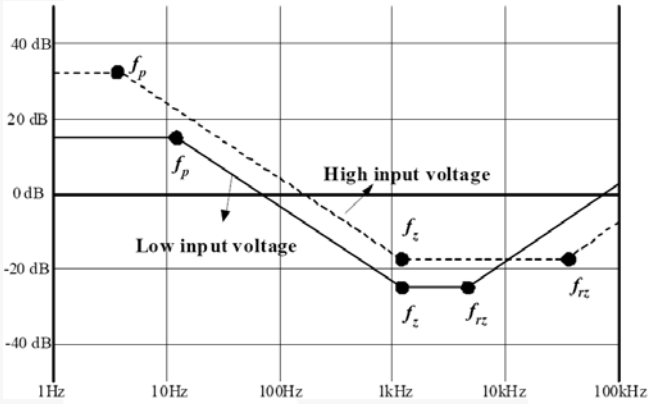

Figure 13. CCM Flyback Converter Control-to-Output Transfer Function Variation for Different Input Voltage

Figure 14 shows the variation of a CCM flyback converter control-to-output transfer function for different loads. Note that the DC gain changes for different loads and the RHP zero is the lowest at the full-load condition.

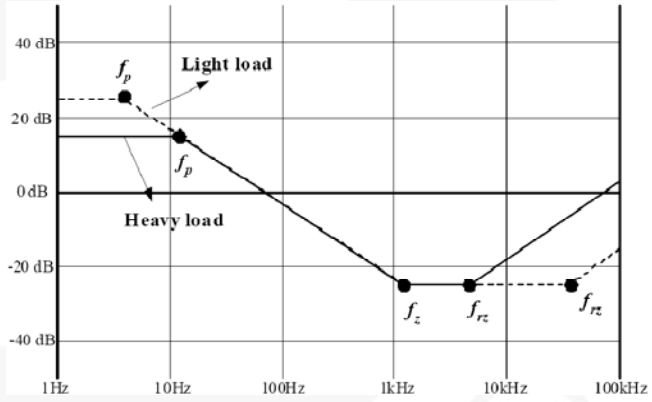

Figure 14. CCM Flyback Converter Control-to-Output Transfer Function Variation for Different Loads

When the input voltage and the load current vary over a wide range, it is not easy to determine the worst case for the feedback loop design. The gain, together with zeros and poles, varies according to the operating conditions. Even though the converter is designed to operate in CCM or at the boundary of DCM and CCM in the minimum input voltage and full-load condition; the converter enters into DCM, changing the system transfer functions as the load current decreases and/or input voltage increases.

One simple and practical way to address this problem is designing the feedback loop for low input voltage and full-load condition with enough phase and gain margin. When the converter operates in CCM, the RHP zero is lowest in low input voltage and full-load condition. The gain increases only about 6dB as the operating condition is changed from the lowest input voltage to the highest input voltage condition under universal input condition. When the operating mode changes from CCM to DCM, the RHP zero disappears, making the system stable. Therefore, by designing the feedback loop with more than 45 degrees of phase margin in low input voltage and full-load condition, the stability over all the operating ranges can be guaranteed.

Figure 15 is a typical feedback circuit mainly consisting of a shunt regulator and a photo-coupler. R_1 and R_2 form a voltage divider for output voltage regulation. R_F and C_F are for control-loop compensation. The maximum source current of the FB pin is about 1mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of R_D, is determined by:

$$\frac{V_O - V_{OPD} - V_{KA}}{R_D} \cdot CTR > I_{FB} \quad (23)$$

where V_{OPD} is the forward-voltage drop of the photodiode (~1.2V); V_{KA} is the minimum cathode-to-anode voltage of KA431 (2.5V); and CTR is the current transfer rate of the opto-coupler.

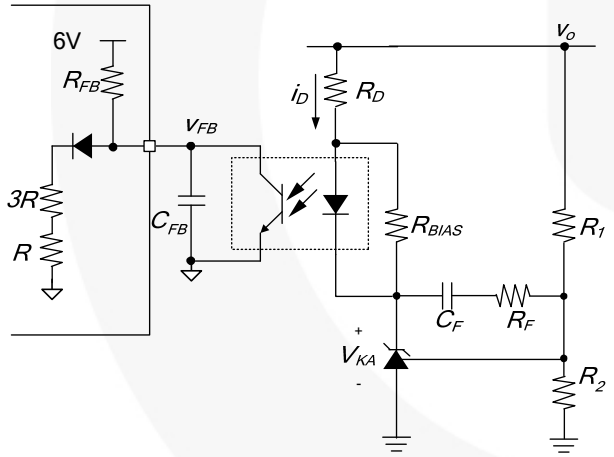

Figure 15. Feedback Circuit

The feedback compensation network transfer function of Figure 15 is obtained as:

$$\frac{\hat{V}_{FB}}{\hat{V}_O} = -\frac{\omega_I}{s} \cdot \frac{1 + s/\omega_{ZC}}{1 + s/\omega_{PC}} \quad (24)$$

where

$$\omega_I = \frac{R_{FB}}{R_1 R_D C_F}, \omega_{ZC} = \frac{1}{(R_F + R_1)C_F} \text{ and } \omega_{PC} = \frac{1}{R_{FB} C_{FB}} \quad (25)$$

(Design Example) Assuming CTR is 100%,

$$\frac{V_O - V_{OPD} - V_{KA}}{R_D} \cdot CTR > 1 \times 10^{-3}$$

$$R_D < \frac{V_O - V_{OPD} - V_{KA}}{1 \times 10^{-3}} = \frac{12 - 1.2 - 2.5}{1 \times 10^{-3}} = 8.3k\Omega$$

The minimum cathode current for KA431 is 1mA.

$R_{BIAS} < \frac{V_{OPD}}{1 \times 10^{-3}} = 1.2k\Omega$.

1kΩ resistor is selected for R_{BIAS}.

The voltage divider resistors R_1 and R_2 should be designed to provide 2.5V to the reference pin of the KA431.The relationship between R_1 and R_2 is given as:

$$R_2 = \frac{2.5 \cdot R_1}{V_O - 2.5} = \frac{2.5 \cdot R_1}{12 - 2.5} = \frac{R_1}{3.8}$$

38.2kΩ and 10kΩ resistor are selected for R_1, R_2.

[STEP-11] Design Input Voltage Sensing Circuit

Figure 16 shows a resistive voltage divider with low-pass filter for line-voltage detection of the VIN pin. FSL-series devices start and enable the latch function when the V_{IN} voltage reaches 1.03V. If latch protection is triggered, the V_{IN} voltage is used for release latch protection as the V_{IN} voltage drops below 0.7V. It is typical to use 100:1 voltage divider for V_{IN} level.

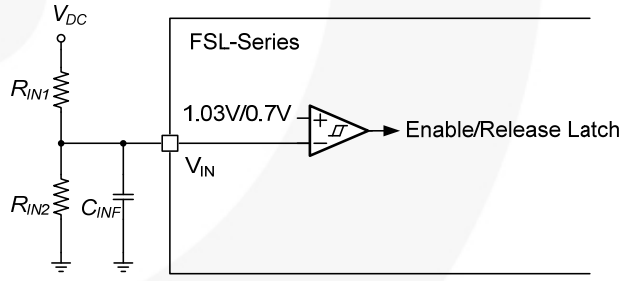

Figure 16. Input Voltage Sensing

4. Printed Circuit Board Layout

High-frequency switching current / voltage makes printed circuit board layout a very important design task. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests.

4.1 Guidelines

To get better EMI performance and reduce line-frequency ripple, the output of the bridge rectifier should be connected to capacitor C_{DC} first, then to the switching circuits.

- The high-frequency current loop is in C_{DC} – Transformer – Drain pin – C_{DC}. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 2→1 in Figure 17) short, direct, and wide. High-voltage traces related the drain and RCD snubber should be kept far away from control circuits to prevent unnecessary interference.
- As indicated by 2, the ground of control circuits should be connected first, then route other traces.
- As indicated by 3, the area enclosed by the transformer auxiliary winding, D_{DD} and C_{DD} should also be kept small. Place C_{DD} close to the controller for good decoupling.
- GND2→3→1 are suggestions for ESD tests where the earth ground is not available on the power supply. In the ESD discharge path, the charge goes from the secondary, through the transformer stray capacitance, to GND3, then GND1, and back to mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common-mode choke (*see Figure 17*) can decrease high-frequency impedance and increase ESD immunity.
- Should a Y-cap between primary and secondary be required, connect this Y-cap to the positive terminal of C_{DC}. If this Y-cap is connected to primary ground, it should be connected to the negative terminal of C_{DC} (GND1) directly. Point discharge of this Y-cap also helps for ESD. In addition, the creepage distance between these two pointed ends should be at least 5mm according to safety requirements.

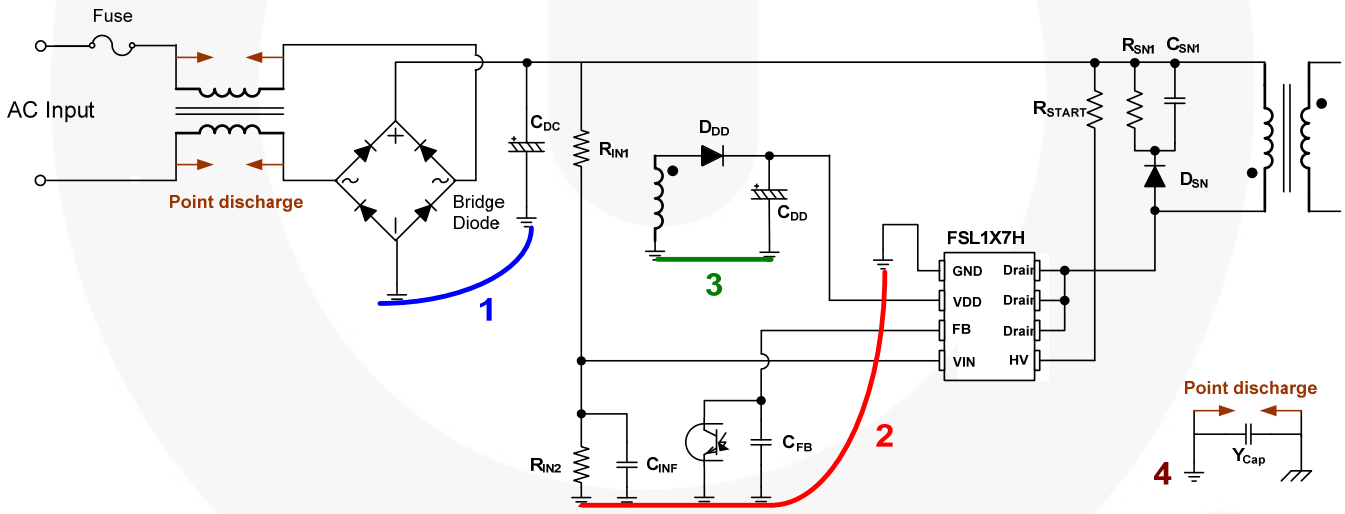

Figure 17. Layout Considerations

5. Design Summary

5.1 Schematic

Figure 18 shows the final schematic of the 12W power supply of the design example.

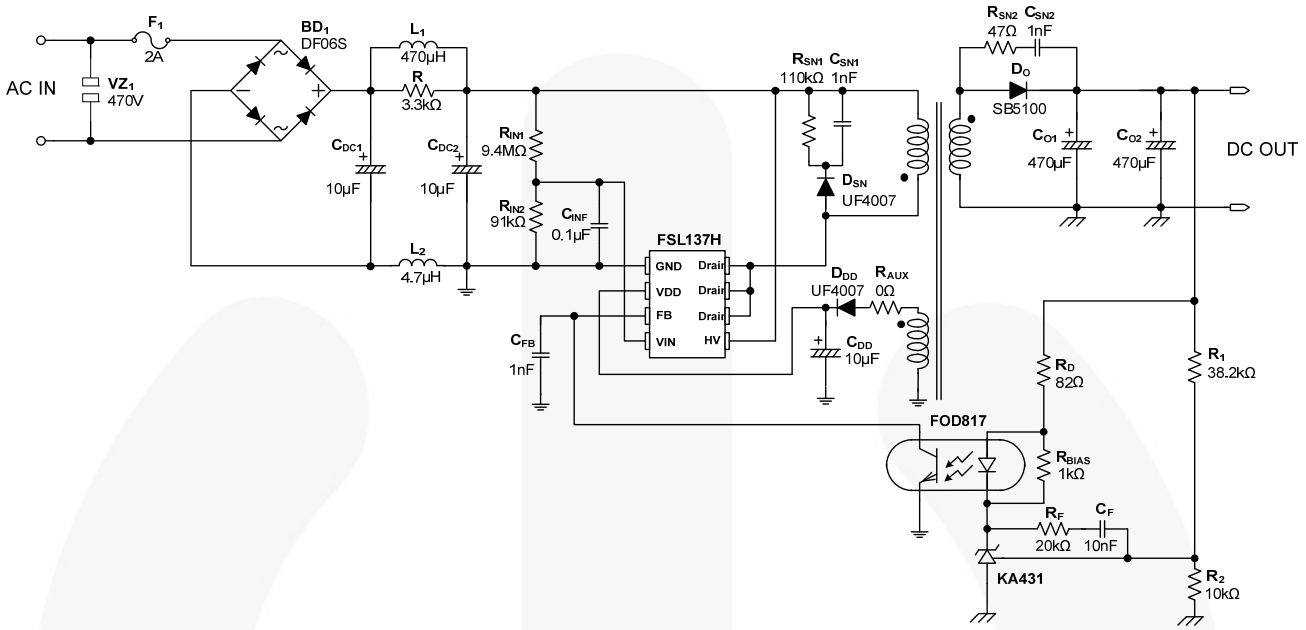

Figure 18. Design Example

5.2 Transformer Specification

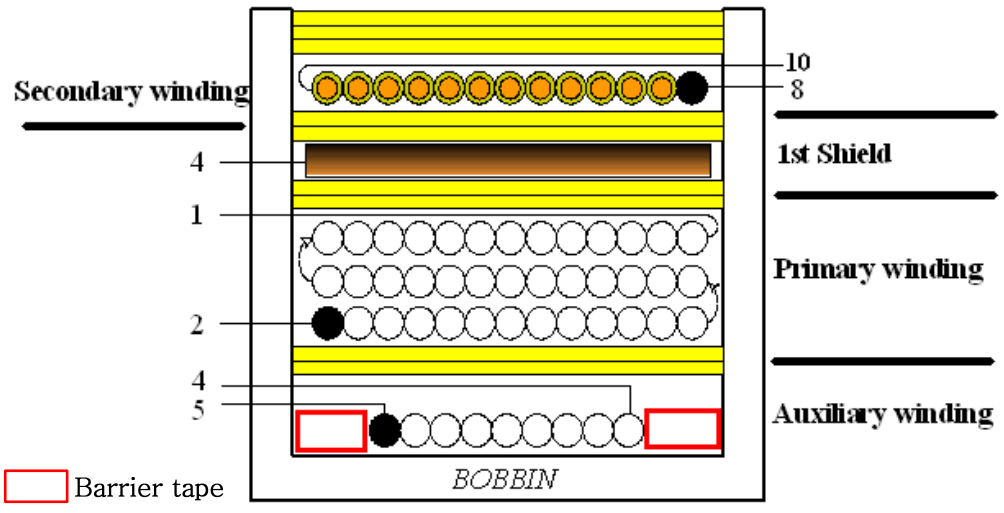

Figure 19.Transformer Specification

- Core: EEL-16 (A_e=19.2mm^2)
- Bobbin: EEL-16

	Pin (S → F)	Wire	Turns
N_a	5 → 4	0.3φ×1	13
Insulation : Polyester Tape t = 0.025mm, 2 Layers			
N_p	2 → 1	0.26φ×1	75
Insulation : Polyester Tape t = 0.025mm, 2 Layers			
-	4 → -	COPPER SHIELD	1.2
Insulation : Polyester Tape t = 0.025mm, 2 Layers			
N_s	8 → 10	0.35φ×1	13
Insulation : Polyester Tape t = 0.025mm, 3 Layers			

	Pin	Specification	Remark
Inductance	1−2	600μH ± 10%	100kHz, 1V
Leakage	1−2	< 30 μH Maximum	Short All Other Pins

Related Resources

FSL127H — Green Mode Fairchild Power Switch (FPS™)
FSL137H— Green Mode Fairchild Power Switch (FPS™)
Fairchild Power Supply WebDesigner — Flyback Design & Simulation - In Minutes at No Expense